UFSOI MOSFET MODELS (Ver. 7.5), Including UFPDB-2.5

User's Guide

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Introduction

Previous versions of UFSOI comprised our *process- and charge-based* NFD and FD SOI compact MOSFET models, which were evolved from basic physical modeling of thin Si-film devices[1]. In UFSOI-6.0, we introduced the UFPDB model (Ver. 1.0), which was evolved by expanding the NFD model to be a *unified*[2] model for partially depleted (PD) SOI and bulk-Si MOSFETs. Because of the process basis of the model, no new model parameters were needed for this expansion. In the PD/SOI mode, UFPDB is equivalent to NFD, which is a five-terminal model[3]. It thus properly accounts for DC as well as dynamic floating-body effects in all regions of operation. In the bulk-Si mode, UFPDB is a four-terminal model with the substrate becoming the body of the MOSFET. It was recently upgraded (Ver. 2.0) to include gate-body tunneling current[4], exchange energy for inversion carriers, a strained Si/SiGe-channel option, and allowance for arbitrary gate dielectric. The strained Si/SiGe option was modified and expanded[5] in UFPDB-2.5, contained in this version of UFSOI (Ver. 7.5). With the upgrades, UFPDB-2.5 is applicable to CMOS devices scaled to the bulk-Si limit (L_{gate} ~ 50nm with L_{eff} ~ 40nm). The UFSOI model for the fully depleted (FD) SOI MOSFET, which physically accounts for the charge coupling between the front and back gates and includes a two-dimensional analysis for the subthreshold region of operation[6], also allows for arbitrary gate dielectric. Both UFSOI models include a quasi-2D accounting for the parasitic (coupled) BJT (current and charge)[7], which can be driven in the floating-body mode by transient body charging current (due to capacitive coupling) and/or thermal generation, GIDL, junction tunneling (in the UFPDB model), and impact-ionization current, the latter of which is characterized by a non-local, carrier temperature-dependent model for the ionization rate integrated across the channel(s), LDD, and drain[8].

1. S. Veeraraghavan and J. G. Fossum, "A Physical Short-Channel Model for the Thin-Film SOI MOSFET Applicable to Device and Circuit CAD," *IEEE Trans. Electron Devices*, vol. 35, pp. 1866-1875, Nov. 1988.
2. M. M. A. Pelella, "Analysis, Modeling, and Control of Floating-Body Effects in Nanometer-Gate-Length Partially Depleted Silicon-on-Insulator CMOS Devices and Circuits," Ph.D. Dissertation, University of Florida, Gainesville, 2000.
3. D. Suh, "Modeling of Non-Fully Depleted Silicon-on-Insulator MOSFETs, and Applications to High-Performance/Low-Power ULSI Design," Ph.D. Dissertation, University of Florida, Gainesville, 1995.
4. J. Yang, "The Modeling of Gate-to-Body Direct Tunneling Current and Its Implementation in UFPDB/Spice3," SOI Group Report, University of Florida, Gainesville, June 2002.
5. W. Zhang and J. G. Fossum, "Strained Si/SiGe Channels: A New Performance Advantage for PD/SOI CMOS," SOI Group Report, University of Florida, Gainesville, Nov. 2002.
6. P. C. Yeh, "Modeling and Design of Deep-Submicron Fully Depleted Silicon-on-Insulator CMOS for Low-Voltage Integrated Circuit Applications," Ph.D. Dissertation, University of Florida, Gainesville, 1996.
7. S. Krishnan, "Analysis and Modeling of Nonlocal and Dynamic Floating-Body Effects for Application in Scaled SOI CMOS Technology," Ph.D. Dissertation, University of Florida, Gainesville, 1996.
8. S. Krishnan, *op cit*.

Previous upgrades in both models include accountings for polysilicon-gate depletion[9], inversion-carrier energy quantization[10], and GIDL/GISL[11]; and, in the UFPDB model, junction tunneling[12] and RSCE/halo effects. Also, a physical accounting for carrier-velocity overshoot[13], or quasi-ballistic transport, was added to both models. The charge modeling[14] is physically linked to the channel-current modeling. All terminal charges (including MOS and bipolar components) and their derivatives are continuous for all bias conditions, as are all currents and their derivatives. Also, SOI substrate depletion charge under the source and drain regions, which becomes important when the back oxide (BOX) is scaled, is included as components of the source, drain, and back-gate charges[15]. For the UFPDB model in the bulk-Si mode, the substrate becomes the well, and this charge reflects the source/drain-junction areal capacitance[16]. Temperature dependence for both models is also implemented[17], without the need for any additional parameters. The temperature-dependence modeling is the basis for the self-heating option[18], which iteratively solves for local device temperature in DC and transient simulations in accord with a user-defined thermal impedance.

Another noteworthy recent improvement is the run-time reduction for the UFPDB model[19]. By switching from finite-difference approximations, which necessitated five calls of the model routine for each Spice call of the model, to approximate analytical derivatives, DC and transient simulation times for the model have been reduced by a factor of 2-3 typically. The difference approximations had to be retained for the V_{BS}-derivatives because of the numerical accuracy required for reliable simulation of floating-body effects. Also, AC simulations still use the difference

9. M.-H. Chiang, "Process-Based Compact Modeling and Analysis of Silicon-on-Insulator CMOS Devices and Circuits, Including Double-Gate MOSFETs," Ph.D. Dissertation, University of Florida, Gainesville, 2001.
10. M.-H. Chiang, *op cit*.
11. K. Kim, "Design and Analysis of Double-Gate CMOS for Low-Voltage Integrated Circuit Applications, Including Physical Modeling of Silicon-on-Insulator MOSFETs," Ph.D. Dissertation, University of Florida, Gainesville, 2001.
12. K. Kim, *op cit*.
13. L. Ge, J. G. Fossum, and B. Liu, "Physical Compact Modeling and Analysis of Velocity Overshoot in Extremely Scaled CMOS Devices and Circuits," *IEEE Trans. Electron Devices*, vol. 48, 2001.
14. D. Chang, "Pragmatic and Reliable Device/Circuit Simulation for Design in Advanced Silicon-Based Technologies," Ph.D. Dissertation, University of Florida, Gainesville, 1997.
15. P. C. Yeh, *op cit*.
16. M. M. A. Pelella, *op cit*.
17. G. O. Workman, J. G. Fossum, S. Krishnan, and M. M. Pelella, "Physical Modeling of Temperature Dependences of SOI CMOS Devices and Circuits Including Self-Heating," *IEEE Trans. Electron Devices*, vol. 45, pp. 125-133, Jan. 1998.
18. D. T. Zweidinger, "Modeling of Transistor Self-Heating for Circuit Simulation," Ph.D. Dissertation, University of Florida, Gainesville, 1997.
19. M.-H. Chiang, *op cit*.

approximations because of the need for accurate derivatives in the definition of the small-signal equivalent circuit.

This User's Guide describes the use of the UFSOI/Ver. 7.5 (UFPDB-2.5 and FD) MOSFET models, which have been implemented and released in a Type-I interface (API)[20] that can be glued to any circuit simulator. The models and the interface, glued to Spice3e2, have been extensively exercised in DC, AC, and transient device and circuit simulations.

UFPDB MOSFET Model

Model Description

The physical UFPDB compact device model is *unified*[21] for PD/SOI[22] and bulk-Si MOSFETs. It is also process- and charge-based, having key parameters that are structurally defined. It has optional accountings for LDD and LDS, or drain/source extensions, as well as the coupled parasitic BJT[23], the latter of which can be influenced by an optional accounting for a halo implant; the halo will also affect threshold voltage similarly to RSCE. UFPDB-2.5 includes an optional accounting for gate-body direct tunneling current[24], valid for all inversion/accumulation conditions, and it accounts for exchange energy in the strongly inverted channel, which tends to lessen the quantization effect on theshold voltage[25]. Further, it includes an expanded option[26] for strained Si-on-$Si_{1-x}Ge_x$ channels in either PD/SOI (SSOI) or bulk-Si MOSFETs, with the Ge content x in the underlying SiGe buffer layer being a new model parameter. The weak-inversion modeling is patterned after that for bulk-Si MOSFETs, but with complete accounting for DC and dynamic floating-body effects. It is linked to the strong-inversion formalism by spline interpolations of current and charge across a physically defined, bias-dependent moderate-inversion region. In the PD/SOI mode, the five-terminal (drain, front gate, source, back gate, and body, which can float) UFPDB model is based on the assumption of a depleted front-surface region, defined for example by a retrograded doping profile in the film body, separated from the BOX by a higher-doped back neutral region. The floating body is a model option, for which the body-source bias is properly characterized by the nodal equation involving the body charging

20. D. M. Newmark, "Simulator Independent MOSFET Model Type-I Standard," Motorola / APRDL Report, Dec. 1995.
21. M. M. A. Pelella, *op cit*.
22. D. Suh, *op cit*.
23. S. Krishnan, *op cit*.
24. J. Yang, *op cit*.
25. J. Yang, *op cit*.
26. W. Zhang and J. G. Fossum, *op cit*.

current as well as carrier generation and recombination currents. In the bulk-Si mode, the model is four-terminal (drain, gate, source, well/substrate), but still based on the same retrograded channel doping profile. The analyses of the (ambipolar) carrier transport in the device structure that underlie the UFPDB model require some minor iterative numerical solution; yet the model is implemented effectively in the API interface, which enables reliable and efficient device/circuit simulation. Approximate analytical derivatives are used predominantly for optimal computational efficiency[27], but finite-difference approximations are still used for the V_{BS}-derivatives as well as for the current and charge derivatives for AC simulations (which means VNTOL should not exceed 1μV). The model routine is hierarchical in that various features are turned on and off by user-specified device- and model-line parameters.

Device Line and Parameters

The general format for specifying the UFPDB MOSFET (in Spice3) is

M*XXXXX* **ND NGF NS** [**NGB**] [**NB**] **MNAME L**=*exp* **W**=*exp* [**M**=*exp*] [**AD**=*exp*] [**AS**=*exp*] [**AB**=*exp*] [**NRD**=*exp*] [**NRS**=*exp*] [**NRB**=*exp*] [**PDJ**=exp] [**PSJ**=exp] [**RTH**=*exp*] [**CTH**=*exp*] [*off*] [**IC** = *Vds*, *Vgfs*, *Vgbs*, *Vbs*]

where the parentheses indicate optional parameters. The device-line parameters are defined as follows.

UFPDB MOSFET Device-Line Parameters

Name	Description	Units	Default
ND	Drain node	-	-
NGF	(Front) gate node	-	-
NS	Source node	-	-
NGB	Back gate (well/substrate) node	-	-
NB	SOI body node	-	-
MNAME	Model name	-	-
L	Gate (polysilicon) length	m	1.0e-6
W	Gate (polysilicon) width	m	1.0e-6
M	Number of gate fingers	-	1
AD	Area of drain region	m^2	0.0
AS	Area of source region	m^2	0.0
AB	Area of body-contact region	m^2	0.0
NRD	Squares of drain region	sq.	0.0
NRS	Squares of source region	sq.	0.0

27. M.-H. Chiang, *op cit*.

NRB	Squares of body-contact region	sq.	0.0
PDJ	Perimeter of drain-body junction	m	W
PSJ	Perimeter of source-body junction	m	W
RTH	Thermal resistance	$K \cdot W^{-1}$	0.0
CTH	Thermal capacitance	$W \cdot s \cdot K^{-1}$	0.0
IC	Initial conditions	V	-

For the PD/SOI mode, five terminals are defined. Omitting NB will float the body. Omitting NGB (which can be done only when NB is omitted) will tie the back gate to ground. For the bulk-Si mode, only four terminals are defined; NGB becomes the well/substrate node, and NB is omitted. Omitting NGB will tie the well/substrate to ground. For floating-body SOI devices, AB is typically zero and should be specified accordingly. For body-contacted devices, AB should be the extrinsic body area. When the self-heating option is activated (on the model line), RTH and CTH, typical values of which are 5e3 and 1e-12, respectively, but which can vary widely from one device to another, are used to define the thermal impedance of the device. For M > 1, W, AD, AS, AB, NRD, NRS, NRB, PDJ, PSJ, RTH, and CTH must be specified per gate finger.

Model Line and Parameters

As noted previously, the UFPDB model parameters are process-based; key parameters relate directly to device structure/physics. Their evaluation[28] can be done and/or facilitated based on knowledge of the technology. The general formats for specifying the UFPDB MOSFET model (in Spice3) are

Model MNAME NMOS LEVEL=10 BODY=1 (2) PARAM1=*value*
PARAM2=*value*.....

Model MNAME PMOS LEVEL=10 BODY=1 (2) PARAM1=*value*
PARAM2=*value*.....

where the complete set of model parameters is shown in the following table (for the nMOS transistor). Some of the parameters are merely flags or other obvious constants, and some optional parameters are allowed.

UFPDB MOSFET Model-Line Parameters

Structural Parameters

Name	Description	Units	Default	Typical
TOXF	(Front-) gate dielectric thickness	m	1.0e-8	3.0e-9

28. M.-H. Chiang, *op cit*.

TOXB	Buried oxide (BOX) thickness	m	0.5e-6	0.2e-6
NSUB	SOI substrate (bulk well/substrate) doping density	cm^{-3} (cm^{-3})	1.0e15 (1.0e17)	1.0e16 (1.0e17)
NGATE	Poly-gate doping density (0 for no poly-gate depletion)	cm^{-3}	0.0	5.0e19
NDS	Source/drain doping density	cm^{-3}	5.0e19	1.0e20
TF	Si-film thickness (source/drain junction depth)	m	0.2e-6	0.2e-6
TB	Effective (depleted) film (channel) thickness	m	0.1e-6	4.0e-8
THALO	Halo thickness (0 for no halo)	m	0.0	0.2e-6
NBL	Low body (channel) doping density	cm^{-3}	5.0e16	5.0e17
NBH	High body doping density	cm^{-3}	5.0e17	1.0e18
NHALO	Halo doping density	cm^{-3}	0.0	2.0e18
LRSCE	Characteristic length for reverse short-channel effect (0 for no RSCE)	m	0.0	0.1e-6
LLDD	LDD region length (0 for no LDD)	m	0.0	5.0e-8
NLDD	LDD doping density (>1e19: LDD/LDS treated as D/S extensions)	cm^{-3}	5.0e19	(>1e19)
DL	Effective channel-length reduction (wrt L)	m	0.0	2.0e-8
DW	Effective channel-width reduction (wrt W)	m	0.0	2.0e-8

Electrical Parameters

Name	Description	Units	Default	Typical
NQFF	Front oxide fixed charge (normalized)	cm^{-2}	0.0	1.0e10
NQFB	Back oxide fixed charge (normalized)	cm^{-2}	0.0	1.0e11
NQFSW	Effective sidewall fixed charge (0 for no narrow-width effect)	cm^{-2}	0.0	
QM	Energy quantization parameter (0 for no quantization nor exchange energy)	-	0.0	1.0
GEX	Ge content in underlying $Si_{1-x}Ge_x$ layer (0 for no strained Si/SiGe channel)	-	0.0	0.20
UO	Low-field (electron/hole) mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$	700./250.	400./200.
THETA	Mobility degradation coefficient	$cm \cdot V^{-1}$	1.0e-6	1.0e-6
VSAT	Carrier saturated drift velocity	$cm \cdot s^{-1}$	7.0e6	7.0e6
VO	Velocity overshoot parameter (0 for no overshoot)	-	0.0	1.0
ALPHA	Impact-ionization coefficient (0 for no impact ionization)	cm^{-1}	0.0	2.45e6

BETA	Impact-ionization exponential factor (0 for no impact ionization)	$V \cdot cm^{-1}$	0.0	1.92e6
BGIDL	Exponential factor for gate-induced drain/source leakage (0 for no GIDL)	$V \cdot m^{-1}$	0.0	4.5e9
NTR	Effective trap density for trap-assisted junction tunneling (0 for no tunneling)	cm^{-3}	0.0	1.0e15
JRO	Body-source/drain junction recombination current coefficient	$A \cdot m^{-1}$	1.0e-10	2.0e-10
M	Body-source/drain junction recombination ideality factor	-	2.0	1.5
LDIFF	Effective diffusion length in source/drain	m	1.0e-7	1.0e-7
SEFF	Effective recombination velocity in source/drain	$cm \cdot s^{-1}$	1.0e5	1.0e-5
KD	Gate dielectric permittivity (relative)	-	3.9	3.9
CGFDO	Gate-drain overlap capacitance	$F \cdot m^{-1}$	0.0	0.5e-9
CGFSO	Gate-source overlap capacitance	$F \cdot m^{-1}$	0.0	0.5e-9
CGFBO	Gate-body overlap capacitance	$F \cdot m^{-1}$	0.0	0.0
RD	Specific drain parasitic resistance	ohm•m	0.0	150.e-6
RS	Specific source parasitic resistance	ohm•m	0.0	150.e-6
RHOB	Body sheet resistance	ohm/sq.	0.0	30.e3
MOX	Electron effective mass (normalized to free electron mass) in gate dielectric (0 for no gate-body tunneling current)	-	0.0	0.36
FNK	Flicker noise coefficient (0 for no flicker noise)	F•A	0.0	
FNA	Flicker noise exponent	-	1.0	

Flag Parameters

Name	Description	Units	Default	Typical
BJT	Parasitic BJT flag (0: off; 1: on)	-	1	1
SELFT	Self-heating flag (0: no self-heating; 1: approximate model; 2: full self-heating)	-	0	0
TPG	Type of gate polysilicon (+1: opposite to body; -1: same as body)	-	1	1
TPS	Type of substrate (+1: opposite to body; -1: same as body)	-	-1	-1/+1

Optional Parameters

Name	Description	Units	Default
VFBF	Front-gate flatband voltage	V	calc.
VFBB	Back-gate flatband voltage	V	calc.
WKF	Front gate-channel (low-doped body) work-function difference	V	calc.
WKB	Back gate-channel (low-doped body) work-function difference	V	calc.
TAUO	Carrier lifetime in lightly doped region	s	calc.
SFACT	Factor for spline smoothing	-	50.0
SVBE	Smoothing parameter for gate-body current in inversion region (0 for no current)	-	13.5
SCBE	Smoothing parameter for (nMOS/pMOS) gate-body current in accumulation region (0 for no current)	-	0.04/0.045
FFACT	Factor for (nMOS/pMOS) gate-body current smoothing in accumulation region	-	0.5/0.8
BFACT	V_{DS}-averaging factor for mobility degradation	-	0.3
FVBJT	BJT current directional partitioning factor (0 for lateral 1D flow)	-	0.0
RB	Total body parasitic resistance	ohm	calc.
RHOSD	Source/drain sheet resistance	ohm/sq.	0.0

The model line must include LEVEL=10, and BODY=1 for the PD/SOI mode or BODY=2 for the bulk-Si mode. For the latter, the following parameters are obviated: TOXB, NQFB, TPS, VFBB, WKB. In this case, NSUB is the bulk-device well/substrate doping density (which defines the source/drain-junction areal capacitance); note that JRO is still a per-unit-width current. Specifying VFBF turns off the narrow-width effect defined by NQFSW (which can be positive or negative) and the reverse short-channel effect defined by LRSCE (and NBH, or NHALO if specified); the latter effect is also turned off when WKF is specified. For body-tied devices, RHOB is used to calculate an effective body resistance based on the device geometry[29]: RB=RHOB(NRB+0.345W/L)/M; this calculation is overridden when RB is specified. For floating-body SOI devices, CGFBO is small and should be specified to be 0. Obviously JRO and SEFF influence the gain of the BJT, but

29. G. O. Workman, *op cit*.

LDIFF affects only bipolar charge storage in the source/drain. The BJT gain is influenced by NBH and NHALO (if THALO is specified) as well. The value of TAUO should generally be loosely correlated with JRO in accord with basic pn-junction recombination/generation properties[30]. Its default value is calculated based on JRO, which is appropriate for short L; for long L, body generation tends to predominate over that in the junctions, and hence an independent TAUO should be specified. When the velocity-overshoot option is used (VO > 0), VSAT should be set to its physical (default) value. The (non-local) impact-ionization model is physical, and its parameters should not be varied arbitrarily. For n-channel devices, the following values have been determined to be generally representative: ALPHA = 2.45e6 and BETA = 1.92e6. GIDL/GISL and junction-tunneling currents can influence the floating-body effects, e.g., on I_{off}. BGIDL and NTR should be hence be defined for PD/SOI devices. These currents are also dependent on the doping-density parameters. The LDD option intensifies the model, so it is advisable to set LLDD to 0 for large-scale circuit simulation, and add the unbiased LDD (and LDS) resistance to RD (and RS); this simplification is foisted when NLDD > 1e19 is specified. For drain/source extensions, set NLDD > 1e19, but specify LLDD for the extension length. For the strained Si-on-SiGe-channel option[31], specify GEX as the Ge content (x) in the underlying $Si_{1-x}Ge_x$ layer. With GEX > 0, the model defines the narrowed energy bandgap in the channel, which implicitly reduces the threshold voltage, and accordingly, with a higher GEX-defined permittivity, modifies the source/drain junction depletion-charge (viz., capacitance) expressions, including peripheral and, for the bulk-Si mode, areal components[32]. These modified features are used in the parasitic BJT formalism as well, and in the GIDL/GISL and drain/source junction-tunneling currents too. Also, in accord with GEX, set UO, VO, and VSAT higher than the respective values for unstrained Si channels, and define THETA, which distinguishes the electron and hole mobilities in strained Si, properly[33]; and BETA should be reduced in accord with the narrowed bandgap. The gate current option (MOX > 0) accounts for only gate-body direct tunneling current (I_{GB})[34] (also affected by the narrowed bandgap in the strained Si/SiGe option), which is only important in floating-body PD/SOI devices. The modeling, valid for all inversion/accumulation conditions, is applicable only for n^+ polysilicon gates on nMOS devices and p^+ polysilicon gates on pMOS devices. The optional parameters SVBE, SCBE,

30. G. O. Workman, *op cit*.
31. W. Zhang and J. G. Fossum, *op cit*.
32. W. Zhang and J. G. Fossum, *op cit*.
33. W. Zhang and J. G. Fossum, *op cit*.
34. J. Yang, *op cit*.

and FFACT are used for smoothing the $I_{GB}(V_{GfS})$ characteristic[35], and generally their default values can be used. Finally, although not generally needed, SFACT can be varied to ensure smooth, or well-behaved (current and charge) spline functions in moderate inversion.

FD/SOI MOSFET Model

Model Description

The physical UFSOI/FD SOI MOSFET compact model[36] is process- and charge-based, having key parameters that are structurally defined. It has optional accountings for LDD and LDS as well as the coupled parasitic BJT[37]. The subthreshold formalism includes a two-dimensional analysis for weak-inversion current, spline interpolations of current and charge across a physically defined, bias-dependent moderate-inversion region linking the weak- and strong-inversion formalisms, and an accounting for fast surface states at the front and back interfaces. The weak-inversion analysis accounts for source/drain field fringing in the BOX and possible current flow in a back channel as well as in the front one. It thereby renders the model valid for deep-submicron FD/SOI devices with arbitrary structure, and even for asymmetrical double-gate (DG) MOSFETs having one predominant channel in strong inversion[38]. The five-terminal (drain, front gate, source, back gate, and body, which normally floats) model is based primarily on the assumption of a (strongly) fully depleted film body, but the formalism has been extended to account for accumulation charge in the body, which can drive dynamic floating-body bipolar effects[39]. The analyses of the (ambipolar) carrier transport in the device structure that underlie the model require some minor iterative numerical solution; yet the model is implemented effectively in the API interface, which enables reliable and efficient device/circuit simulation. Finite-difference approximations are used for the current and charge derivatives (which means VNTOL should never exceed 1μV). The model routine is hierarchical in that various features are turned on and off by user-specified device- and model-line parameters.

Device Line and Parameters

The general format for specifying the FD/SOI MOSFET (in Spice3) is

35. J. Yang, *op cit*.
36. P. C. Yeh, *op cit*.
37. S. Krishnan, *op cit*.
38. Y. Chong, "A Preliminary Simulation-Based Assessment of Double-Gate CMOS Devices and Circuits," M.S. Thesis, University of Florida, Gainesville, 1998.
39. D. Chang, *op cit*.

M*XXXXX* **ND NGF NS** [**NGB**] [**NB**] **MNAME L**=*exp* **W**=*exp* [**M**=*exp*] [**AD**=*exp*]
[**AS**=*exp*] [**AB**=*exp*] [**NRD**=*exp*] [**NRS**=*exp*] [**NRB**=*exp*] [**PDJ**=exp]
[**PSJ**=exp] [**RTH**=*exp*] [**CTH**=*exp*] [*off*] [**IC** = *Vds*, *Vgfs*, *Vgbs*, *Vbs*]

where the parentheses indicate optional parameters. The device-line parameters are defined as follows.

FD/SOI MOSFET Device-Line Parameters

Name	Description	Units	Default
ND	Drain node	-	-
NGF	Front gate node	-	-
NS	Source node	-	-
NGB	Back gate node	-	-
NB	Body node	-	-
MNAME	Model name	-	-
L	Gate (polysilicon) length	m	1.0e-6
W	Gate (polysilicon) width	m	1.0e-6
M	Number of gate fingers	-	1
AD	Area of drain region	m^2	0.0
AS	Area of source region	m^2	0.0
AB	Area of body-contact region	m^2	0.0
NRD	Squares of drain region	sq.	0.0
NRS	Squares of source region	sq.	0.0
NRB	Squares of body-contact region	sq.	0.0
PDJ	Perimeter of drain-body junction	m	W
PSJ	Perimeter of source-body junction	m	W
RTH	Thermal resistance	$K \cdot W^{-1}$	0.0
CTH	Thermal capacitance	$W \cdot s \cdot K^{-1}$	0.0
IC	Initial conditions	V	-

Omitting NGB (which can be done only when NB is omitted) will tie the back gate to ground. Omitting NB will float the body. For floating-body devices, AB is typically zero and should be specified accordingly. For body-contacted devices, AB should be the extrinsic body area. When the self-heating option is activated (on the model line), RTH and CTH, typical values of which are 5e3 and 1e-12, respectively, but which can vary widely from one device to another, are used to define the thermal impedance of the device. For M > 1, W, AD, AS, AB, NRD, NRS, NRB, PDJ, PSJ, RTH, and CTH must be specified per gate finger.

Model Line and Parameters

As noted previoulsy, model parameters are process-based; key parameters relate directly to device structure/physics. Parameter evaluation[40] can thus be done and/or facilitated based on knowledge of the SOI technology. The general formats for specifying the charge-based FD/SOI MOSFET model (in Spice3) are

Model MNAME NMOS LEVEL=10 BODY=0 PARAM1=*value* **PARAM2**=*value*.....

Model MNAME PMOS LEVEL=10 BODY=0 PARAM1=*value* **PARAM2**=*value*.....

where the complete set of model parameters is shown in the following table (for the nMOS transistor). Note that some parameters are merely flags or other obvious constants, and that some optional parameters are allowed.

FD/SOI MOSFET Model-Line Parameters

Structural Parameters

Name	Description	Units	Default	Typical
TOXF	(Front-) gate dielectric thickness	m	1.0e-8	1.0e-9
TOXB	Buried oxide thickness	m	0.5e-6	0.2e-6
NSUB	Substrate doping density	cm^{-3}	1.0e15	1.0e16
NGATE	Poly-gate doping density	cm^{-3}	0.0	
	(0 for no poly-gate depletion)			
NDS	Source/drain doping density	cm^{-3}	5.0e19	1.0e20
TB	Si-film (body) thickness	m	0.1e-6	5.0e-8
NBODY	Body doping density	cm^{-3}	5.0e16	1.0e15
LLDD	LDD region length (0 for no LDD)	m	0.0	0.0
NLDD	LDD doping density	cm^{-3}	5.0e19	
	(>1e19: LDD/LDS treated as D/S extensions)			
DL	Effective channel-length reduction (wrt L)	m	0.0	2.0e-8
DW	Effective channel-width reduction (wrt W)	m	0.0	2.0e-8

Electrical Parameters

Name	Description	Units	Default	Typical
NQFF	Front oxide fixed charge (normalized)	cm^{-2}	0.0	1.0e10
NQFB	Back oxide fixed charge (normalized)	cm^{-2}	0.0	1.0e11

40. M.-H. Chiang, *op cit*.

NQFSW	Effective sidewall fixed charge (0 for no narrow-width effect)	cm^{-2}	0.0	
NSF	Front surface-state density	$cm^{-2} \cdot eV^{-1}$	0.0	1.0e10
NSB	Back surface-state density	$cm^{-2} \cdot eV^{-1}$	0.0	1.0e11
QM	Energy quantization parameter (0 for no quantization)	-	0.0	1.0
UO	Low-field (electron/hole) mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$	700./250.	1300./450.
THETA	Mobility degradation coefficient	$cm \cdot V^{-1}$	1.0e-6	1.0e-6
VSAT	Carrier saturated drift velocity	$cm \cdot s^{-1}$	7.0e6	7.0e-6
VO	Velocity overshoot parameter (0 for no overshoot)	-	0.0	1.0
ALPHA	Impact-ionization coefficient (0 for no impact ionization)	cm^{-1}	0.0	2.45e6
BETA	Impact-ionization exponential factor (0 for no impact ionization	$V \cdot cm^{-1}$	0.0	1.92e6
BGIDL	Exponential factor for gate-induced drain leakage (0 for no GIDL)	$V \cdot m^{-1}$	0.0	4.5e9
GAMMA	BOX fringing field weighting factor	-	0.3	0.5
KAPPA	BOX fringing field weighting factor	-	0.5	0.7
JRO	Body-source/drain junction recombination current coefficient	$A \cdot m^{-1}$	1.0e-10	1.0e-10
M	Body-source/drain junction recombination ideality factor	-	2.0	1.5
LDIFF	Effective diffusion length in source/drain	m	1.0e-7	1.0e-7
SEFF	Effective recombination velocity in source/drain	$cm \cdot s^{-1}$	1.0e5	1.0e5
KD	(Front-) gate dielectric permittivity (relative)	-	3.9	3.9
CGFDO	Gate-drain overlap capacitance	$F \cdot m^{-1}$	0.0	0.5e-9
CGFSO	Gate-source overlap capacitance	$F \cdot m^{-1}$	0.0	0.5e-9
CGFBO	Gate-body overlap capacitance	$F \cdot m^{-1}$	0.0	
RD	Specific drain parasitic resistance	ohm•m	0.0	200.e-6
RS	Specific source parasitic resistance	ohm•m	0.0	200.e-6
RHOB	Body sheet resistance	ohm/sq.	0.0	
FNK	Flicker noise coefficient (0 for no flicker noise)	F•A	0.0	
FNA	Flicker noise exponent	-	1.0	

Flag Parameters

Name	Description	Units	Default	Typical
BJT	Parasitic BJT flag (0: off; 1: on)	-	1	1
SELFT	Self-heating flag (0: no self-heating; 1: approximate model; 2: full self-heating)	-	0	0
TPG	Type of gate polysilicon (+1: opposite to body; -1: same as body)	-	1	
TPS	Type of substrate (+1: opposite to body; -1: same as body)	-	-1	-1/+1

Optional Parameters

Name	Description	Units	Default
VFBF	Front-gate flatband voltage	V	calc.
VFBB	Back-gate flatband voltage	V	calc.
WKF	Front gate-channel work-function difference	V	calc.
WKB	Back gate-channel work-function difference	V	calc.
TAUO	Carrier lifetime in lightly doped region	s	calc.
BFACT	V_{DS}-averaging factor for mobility degradation	-	0.3
FVBJT	BJT current directional partitioning factor (0 for lateral 1D flow)	-	0.0
RB	Total body parasitic resistance	ohm	calc.
RHOSD	Source/drain sheet resistance	ohm/sq.	0.0

The model card must include LEVEL=10 and BODY=0. NQFF and NQFB include the flatband charge on the front and back surface states. Specifying VFBF turns off the narrow-width effect defined by NQFSW (which can be positive or negative). For floating-body devices, CGFBO is small and should be specified to be 0. The gain of the parasitic BJT can be effectively tuned by varying JRO and SEFF; LDIFF controls only the bipolar charge stored in the source/drain. (FVBJT is not generally needed, but its value (between 0 and 1) can be tuned for drain-source breakdown in some devices.) The value of TAUO should generally be loosely correlated with JRO in accord with basic pn-junction recombination/generation properties[41]. Its default value is calculated based on JRO, which is appropriate for short L; for long L, body generation tends to predominate

41. G. O. Workman, *op cit*.

over that in the junctions, and hence an independent TAUO should be specified. When the velocity-overshoot option is used (VO > 0), VSAT should be set to its physical (default) value. Since the (non-local) impact-ionization model is physical, its parameters should not be varied arbitrarily. For n-channel devices, the following values have been determined to be generally representative: ALPHA = 2.45e6 and BETA = 1.92e6. GIDL/GISL current can influence I_{off} of the FD device; BGIDL, typically 2-5e9, should be set accordingly. Proper values of KAPPA and GAMMA correlate with TOXB[42]. For example, for common thick BOX (TOXB ~ 200nm), KAPPA = 0.7 and GAMMA = 0.5; for DG MOSFETs with thin TOXB ~ TOXF, KAPPA = GAMMA = 1.0. Since the LDD option intensifies the model, it is advisable to set LLDD to 0 for large-scale circuit simulation, and add the unbiased LDD (and LDS) resistance to RD (and RS); this simplification is foisted when NLDD > 1e19 is specified.

UFSOI Model Parameter Evaluation

The UFSOI models are process-based. As categorized in the UFPDB and FD/SOI model descriptions, the key parameters are structural or electrical, and can (should) be evaluated based on device structure and physics[43]. Superficial knowledge of the structure quickly leads to a preliminary model card, and then tuning of only a few key parameters via minimal measured data is necessary to complete a reliable calibration. Extensive optimization is not required. It is imperative that proper values[44] of the physical model parameters are used; use of unrealistic values can result in convergence problems as well as invalid simulations. For large SOI circuit simulation, certain model options should be used or not used strategically. For example, turning off self-heating, impact ionization, and the parasitic BJT can improve convergence dramatically as well as reduce run time substantively; but these options may be needed for some devices, depending on the circuit being analyzed.

42. P.C. Yeh, *op cit*.
43. M.-H. Chiang, *op cit*.
44. M.-H. Chiang, *op cit*.